CLAIMS

What is claimed is:

1. A method of testing a programmable logic device to determine whether the programmable logic device is functional when configured to instantiate a circuit design expressed in a design database, wherein the programmable logic device includes a plurality of logic blocks and programmable interconnect resources, the method comprising:
   a. identifying a collection of signal paths defined in the design database, each signal path including a source node and a destination node;
   b. instantiating the signal paths on the programmable logic device;
   c. testing the instantiated signal paths to identify a failed signal path;
   d. correlating the failed signal path with at least one alternative signal path extending between the source and destination nodes of the failed signal path;
   e. instantiating the alternative signal path on the programmable logic device; and
   f. testing the instantiated alternative signal path.

2. The method of claim 1, wherein testing the instantiated alternative signal path includes:
   a. configuring one of the logic blocks as a test-signal generator;
   b. issuing a test signal from the configured logic block; and
   c. transmitting the test signal through the instantiated alternative signal path.

3. The method of claim 2, wherein testing the instantiated alternative signal path includes configuring a second of the logic blocks as a test-signal observer, the test-signal observer receiving the test signal from the test-signal generator via the instantiated alternative signal path.

4. The method of claim 1, wherein the logic blocks are programmable.

5. The method of claim 1, further comprising:
   a. identifying a set of logical functions specified in the design database; and
   b. correlating each of the logical functions with a plurality of alternate ones of the logic blocks capable of performing the logical function.

6. The method of claim 5, further comprising, for each logical function:
   a. programming one of the plurality of alternate ones of the logic blocks to perform the logical function;
   b. testing the programmed one of the plurality of alternate ones of the logic blocks to identify a failed logic block;
   c. programming a second of the plurality of alternate ones of the logic blocks to perform the logical function; and
   d. testing the programmed second of the plurality of alternate ones of the logic blocks to verify performance of the logical function.

7. A method of verifying the functionality of a design specified for instantiation on a programmable logic device, the programmable logic device including programmable blocks selectively interconnectable by a collection of programmable interconnect resources, the method comprising:
   a. identifying a plurality of the programmable blocks required for the design, the programmable blocks including signal source nodes and signal destination nodes;
   b. identifying a plurality of the interconnect resources required for the design to interconnect the signal source nodes to respective signal destination nodes,

the plurality of interconnect resources including alternative resources for interconnecting signal source nodes and signal destination nodes;

c. configuring at least a selected one of the plurality of programmable blocks to provide a signal-generation function, wherein the design specifies a second function different from the signal-generation function for the selected one of the plurality of programmable blocks; and

d. identifying functional and defective ones of the plurality of interconnect resources interconnecting signal source nodes and signal destination nodes.

8. The method of claim 7, wherein identifying functional and defective ones of the plurality of interconnect resources comprises:

a. configuring a second selected one of the plurality of programmable blocks to provide a test-signal-observer; and

b. alternatively connecting the programmable block configured to provide a signal-generation function to the second programmable block configured to provide a test-signal-observer function via the alternative resources.

9. The method of claim 8, further comprising sending a test signal from the programmable block configured to provide a signal-generation function to the second programmable block configured to provide a test-signal-observer function.

10. The method of claim 9, further comprising sending the test signal repeatedly over alternative interconnect resources.

11. The method of claim 8, further comprising reading the state of the second programmable block.

12. The method of claim 7, wherein the programmable blocks include at least one of logic blocks, input/output blocks, and memory blocks.

13. The method of claim 7, wherein the programmable blocks are fabricated with a first minimum feature size and the interconnect resources are fabricated with a second minimum feature size less than the first minimum feature size.

14. A computer-readable medium having computer-executable instructions for performing the steps of:
    a. receiving an expression for a customer design for instantiation on a programmable logic device;
    b. identifying a plurality of configurable interconnect resources on the programmable logic device required for the design; and
    c. generating alternative test designs expressing alternative configurations of the interconnect resources based upon the expression for the customer design.

15. The computer-readable medium of claim 14, wherein generating alternative test designs comprises specifying alternative signal paths between corresponding source/destination signal nodes.

16. The computer-readable medium of claim 15, further comprising instructions for testing a plurality of the alternative signal paths for a selected pair of source/destination signal nodes.

17. The computer-readable medium of claim 16, further comprising instructions for storing data correlating a functional one of the alternative signal paths to a corresponding pair of source/destination signal nodes.

18. The computer-readable medium of claim 14, wherein the alternative test designs use substantially all of the programmable resources required for the customer design.

19. The computer-readable medium of claim 14, further including computer-executable instructions for:
    a. identifying a plurality of logic functions specified in the user design; and
    b. identifying, for each logic function, at least two alternative programmable blocks capable of performing the logic function.

20. A method of testing a programmable logic device to determine whether the programmable logic device is functional when configured to instantiate a circuit design expressed in a design database, wherein the programmable logic device includes a plurality of logic blocks and programmable interconnect resources, the interconnect resources having a minimum feature size of at most ten nanometers, the method comprising:
    a. identifying a collection of signal paths defined in the design database, each signal path including a source node and a destination node;
    b. instantiating the signal paths on the programmable logic device;
    c. testing the instantiated signal paths to identify a failed signal path;
    d. correlating the failed signal path with at least one alternative signal path extending between the source and destination nodes;
    e. instantiating the alternative signal path on the programmable logic device; and
    f. testing the instantiated alternative signal path.

21. The method of claim 20, wherein testing the instantiated alternative signal path includes:
    a. configuring one of the logic blocks as a test-signal generator;
    b. issuing a test signal from the configured logic block; and
    c. transmitting the test signal through the instantiated alternative signal path.

22. The method of claim 21, wherein testing the instantiated alternative signal path includes configuring a second of the logic blocks as a test-signal observer, the test-signal observer receiving the test signal from the test-signal generator via the instantiated alternative signal path.

23. The method of claim 20, wherein the logic blocks have a second minimum feature size greater than the first-mentioned minimum feature size.

24. The method of claim 23, wherein the first-mentioned minimum feature size is less than 10% of the second minimum feature size.

25. The method of claim 20, further comprising:
    a. identifying a set of logical functions specified in the design database; and
    b. correlating each of the identified logical functions with a plurality of alternate ones of the logic blocks capable of performing the logical function.

26. The method of claim 25, further comprising, for each logical function:
    a. programming one of the plurality of alternate ones of the logic blocks to perform the logical function;
    b. testing the programmed one of the plurality of alternate ones of the logic blocks to identify a failed

logic block;

c. programming a second of the plurality of alternate ones of the logic blocks to perform the logical function; and

d. testing the programmed second of the plurality of alternate ones of the logic blocks to verify performance of the logical function.

27. The method of claim 20, further comprising specifying a plurality of auxiliary resources unlisted in the design database.

28. The method of claim 27, further comprising testing the auxiliary resources.

29. The method of claim 28, wherein testing the auxiliary resources identifies passing auxiliary resources, the method further comprising sending a customer the programmable logic device and a list of the passing auxiliary resources.

30. The method of claim 28, further comprising rejecting the programmable logic device for use with the circuit design based upon a failure of at least one of the plurality of auxiliary resources.

31. A method of testing a programmable logic device to determine whether the programmable logic device is functional when configured to instantiate first and second circuit designs expressed in respective first and second design expressions, wherein the programmable logic device includes a plurality of logic blocks and programmable interconnect resources, the interconnect resources having a minimum feature size, the method comprising:

a. merging the first and second design expressions into a merged design expression;

b. identifying a collection of signal paths defined in the

merged design expression, each signal path including a source node and a destination node;

c. instantiating the signal paths on the programmable logic device; and

d. testing the instantiated signal paths to identify a failed signal path.

32. The method of claim 31, wherein the minimum feature size is at most ten nanometers.

33. The method of claim 31, further comprising correlating the failed signal path with at least one alternative signal path extending between the source and destination nodes.

34. The method of claim 31, further comprising instantiating the alternative signal path on the programmable logic device.

35. The method of claim 31, further comprising testing the instantiated alternative signal path.

36. The method of claim 31, further comprising specifying a plurality of auxiliary resources unlisted in the design expressions.

37. The method of claim 35, further comprising testing the auxiliary resources.

38. The method of claim 36, wherein testing the auxiliary resources identifies passing auxiliary resources, the method further comprising sending a customer the programmable logic device and a list of the passing auxiliary resources.

39. The method of claim 36, further comprising rejecting the programmable logic device for use with the circuit design based upon a failure of at least one of the plurality of auxiliary resources.

40. A method of testing a programmable logic device to determine whether the programmable logic device is functional when configured to instantiate a circuit designs expressed in a design expression, wherein the programmable logic device includes a plurality of logic blocks and programmable interconnect resources, the method comprising:
    a. identifying a collection of signal paths defined in the design expression, each signal path including a source node and a destination node;
    b. specifying a plurality of auxiliary resources unlisted in the design expression;
    c. instantiating the signal paths on the programmable logic device; and
    d. testing the instantiated signal paths and the auxiliary resources.

41. The method of claim 39, wherein testing the auxiliary resources identifies passing auxiliary resources, the method further comprising sending a customer the programmable logic device and a list of the passing auxiliary resources.

42. The method of claim 40, further comprising rejecting the programmable logic device for use with the circuit design based upon a failure of at least one of the plurality of auxiliary resources.

43. The method of claim 39, wherein the testing identifies a failed signal path, the method further comprising correlating the failed signal path with at least one alternative signal path extending between the respective source and destination nodes.

44. The method of claim 42, further comprising instantiating the alternative signal path on the programmable logic device.

45. The method of claim 43, further comprising testing the instantiated alternative signal path.